APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,195	02/25/2004	Alexander G. MacInnis	13398US02	2398

23446   7590   11/25/2008
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ART UNIT	PAPER NUMBER
2193	

MAIL DATE	DELIVERY MODE
11/25/2008	PAPER

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Application Number: 10/786,195
Filing Date: February 25, 2004
Appellant(s): MACINNIS ET AL.

John A. Wiberg
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 06 October 2008 appealing from the Office action mailed 07 December 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,659,780   WU   8-1997

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-27 stand rejected under 35 U.S.C. 102(b) as being anticipated by Wu.

Relative to claims 1, 10 and 19, Wu's Fig. 1 illustrates a media (note column 1, lines 13-15 and 35-38) processing filter (note column 2, lines 17-20) engine including a first memory unit (multi-port memory M and the topmost output port that feeds rs21) a second memory unit (multi-port memory M and the middle output port that feeds rs11) and a single instruction, multiple data, SIMD, processor (note column 1, lines 54-56 and the abstract).

Relative to claims 10 and 19, the claimed first and second shift registers correspond to Wu's Fig. 1 shift registers rs21 and rs11, respectively. Relative to the recited selective shifting by a predetermined number of bits corresponding to the size of the data element note that when Wu's shift register receive the shift/load control signal 1 (column 3, lines 37-38) the loaded data is shifted the number of bits that correspond to the data size. Relative to claim 19, wherein the shift is described as a multiple of the data size note that 1 is a multiple.

Relative to the recited non-split operation mode, e.g. claim 2, note that Wu's Fig. 20 illustrates receiving of data from only one of the first and second memory units.

Relative to the recited first and second sets of data paths, e.g. claim 5, note the processing elements of Wu's Fig. 1.

(10) Response to Argument

Contrary to appellant's remarks, Wu's multi-port memory M may be view as being multiple memory units because the plurality of data that is stored in M is stored in a plurality of

storage locations or memory units. Also, associating an output port with M defines one memory

unit and associating another output port with M defines another memory unit.

Contrary to appellant's remarks, Wu clearly processes media data, note column 1, lines

13-15 and 35-37 where the data is described as "video image" and "television" which is media

data.

Contrary to appellant's remarks, Wu's shift registers shift their contents by a

predetermined number of bits corresponding to the size of a data element when they receive the

shift/load control signal 1, note column 3, lines 37-38. Relative to the term "multiple" note that

"1" is a multiple.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related

Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejection should be sustained.

Respectfully submitted,

/David H. Malzahn/

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